What is claimed is:

1. A semiconductor integrated circuit device including a nonvolatile semiconductor memory, the device comprising:

a semiconductor substrate having a main surface;

at least one pair of laminating structure bodies formed on the main surface of said semiconductor substrate to be adjacent to each other, each laminating structure body comprising a first gate insulating film, a floating gate electrode, a second gate insulating film, a control gate electrode, and a first protection insulating film having an etching prevention film on both sidewall portions thereof, and being laminated in this order;

a first impurity introduced region which is formed on the main surface of said semiconductor substrate located between sidewall portions facing each other in said one pair of laminating structure bodies, and which functions as one of a source region and a drain region;

a second protection insulating film formed to cover the respective sidewall portions of said one pair of laminating structure bodies, and having a bottom portion extending on one surface portion of said first impurity introduced region; and

a first conductive layer which is formed to fill a connection hole defined by said second protection insulating film covering said sidewall portions facing each other in said one pair of laminating structure body, and which is electrically connected to said first impurity introduced region.

2. The semiconductor integrated circuit device according to claim 1,

wherein said first gate insulating film comprises a silicon oxide film, and at least one part of said first protection insulating film includes a silicon oxide film, and said etching prevention film and said second protection insulating film consist of a silicon nitride film.

3. The semiconductor integrated circuit device according to claim 2,

wherein said first protection insulating film comprises a silicon oxide film and a silicon nitride film laminated on an upper portion thereof.

4. The semiconductor integrated circuit device according to claim 1,

wherein said first impurity introduced region functions as a drain region, and said first conductive layer functions as a part of a data line.

5. The semiconductor integrated circuit device according to claim 4,

wherein an interlayer insulating film consisting of at least one layer of a silicon oxide film is formed on upper portions of said at least one pair of laminating structure bodies, and said data line is formed over said interlayer insulating film.

6. The semiconductor integrated circuit device according to claim 4,

wherein a second impurity region functioning as a source region is formed on the main surface of said semiconductor substrate located at sidewall portions opposite to the sidewall portions which said one pair of laminating structure bodies has

and between which said first impurity introduced region is formed, and

wherein a second conductive layer functioning as a part of a source line is electrically connected to said second impurity region.

7. The semiconductor integrated circuit device according to claim 6,

wherein said second conductive layer functioning as said source region is formed to fill a connection hole defined by said second protection insulating film covering said sidewall portions facing each other in said one pair of laminating structure bodies between which said second impurity region is put.

8. The semiconductor integrated circuit device according to claim 1,

wherein said second gate insulating film consists of an insulating film having a structure of at least three layers formed by laminating alternately a silicon oxide film and a silicon nitride film.

9. The semiconductor integrated circuit device according to claim 1,

wherein each of said at least one pair of laminating structure bodies constitutes a memory cell of a flash memory, and writing into said memory cell is carried out by injecting a charge into said floating gate electrode.

10. The semiconductor integrated circuit device according to claim 9,

~~wherein said flash memory is an NOR type flash memory.~~

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11. A method for manufacturing a semiconductor integrated circuit device including a MIS transistor structure, the method comprising the steps of:

(a) forming a first gate insulating film for forming the MIS transistor structure on a main surface of a semiconductor substrate;

(b) forming at least one pair of laminating structure bodies each including two layers of a first gate electrode covering a part of said first gate insulating film and a first insulating film covering said first gate electrode, an etching prevention film being formed on a sidewall portion of said first insulating film;

(c) introducing impurities into said semiconductor substrate through said first gate insulating film located in a region uncovered with said laminating structure bodies, and thereby forming a first impurity introduced region self-aligned with said laminating structure bodies on the main surface of said semiconductor substrate.

(d) removing said first gate insulating film in the region uncovered with said laminating structure bodies after said step (c); and

(e) forming a second insulating film covering upper portions and sidewall portions of said laminating structure bodies after said step (d).

2. ~~12.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~11~~ 1, further

comprising a step of:

(d-2) oxidizing the main surface of said semiconductor substrate in a region from which said first gate insulating film is removed, and thereby forming an insulating film on said main surface, between said steps (d) and (e).

3. ~~13.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~12~~ 2, further comprising the steps of:

(f) forming a third insulating film over said second insulating film so as to cover said laminating structure bodies covered with said second insulating film and to embed each space between said laminating structure bodies; and

(g) forming a mask for a contact hole over said third insulating film, and selectively removing said third insulating film and said second insulating film in a laminating direction thereof by anisotropic etching using said mask, and thereby forming the contact hole which penetrates said third insulating film and said second insulating film and which reaches a surface of said first impurity introduced region.

4. ~~14.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~13~~ 3, further comprising a step of:

(h) forming a wiring conductive layer embedding said contact hole and electrically connected to said first impurity introduced region, after said step (g).

5. ~~15.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~14~~ 4,

wherein a second gate insulating film and a second gate electrode laminated on an upper portion thereof are interposed between said first gate electrode and said first insulating film constituting each of said laminating structure bodies.

6. ~~16.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~14~~ 4,

wherein said first gate insulating film, said first insulating film and said third insulating film each consist of a silicon oxide film, and said etching prevention film and said second insulating film each consist of a silicon nitride film.

7. ~~17.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~16~~ 6,

wherein said first gate electrode and said second gate electrode consist of a polycrystalline silicon film, and said second gate insulating film consists of a three-layer film in which a silicon oxide film, a silicon nitride film and a silicon oxide film are laminated in this order.

8. ~~18.~~ The method for manufacturing a semiconductor integrated circuit device according to claim ~~17~~ 7,

wherein said first insulating film consists of a two-layer film in which a silicon oxide film and a silicon nitride film are laminated in this order, and said etching prevention film is formed to cover a sidewall portion of said two-layer film.

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19. ~~A~~ method for manufacturing a semiconductor integrated circuit ~~device~~, comprising the steps of:

(a) forming, on a ~~main~~ surface of a semiconductor substrate, a first gate insulating film consisting of a silicon

oxide film, and forming a first conductive film, a second gate insulating film and a second conductive film over said first gate insulating film in this order;

(b) forming a first protection insulating film consisting of one of a single layer film and a laminating film, said single layer film being a silicon oxide film formed over said second conductive film, and said laminating film being a silicon nitride film formed over the silicon oxide film;

(c) patterning said first protection insulating film, and thereby forming an etching mask consisting of said first protection insulating film;

(d) patterning said second conductive film, said second gate insulating film and said first conductive film in this order by dry etching using said etching mask as a mask, and thereby forming a plurality of gate electrodes that each have a floating gate electrode consisting of said first conductive film and a control gate electrode consisting of said second conductive film and that each have a laminating structure in which an upper portion of said control gate electrode is covered with said first protection insulating film;

(e) forming a etching prevention film consisting of a silicon nitride film on both sidewall portions of said first protection insulating film patterned, after said step (c) and before said step (d), or after said step (d);

(f) introducing impurities into the main surface of said semiconductor substrate located between sidewall portions facing each other in said plurality of gate electrodes, and

thereby forming a source region and a drain region;

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(g) treating a surface of said semiconductor substrate by using etchant containing a hydrofluoric acid after said step (f), and thereby cleaning said first gate insulating film located between the sidewall portions which face each other in said plurality of gate insulating film;

(h) covering an upper portion and both sidewall portions of each of said plurality of gate electrodes after said step (g), and forming a second protection insulating film consisting of a silicon nitride film having such a thickness as to partially embed a region between the sidewall portions which face each other in said plurality of gate electrodes;

(i) forming, on an upper portion of said second protection insulating film, an interlayer insulating film consisting of a silicon oxide film, and embedding, with said interlayer insulating film, the region between the sidewall portions which face each other in said plurality of gate electrodes;

(j) etching said interlayer insulating film and said second protection insulating film located between the sidewall portions which face each other in said plurality of gate electrodes, and thereby forming a first connection hole for exposing a surface of said source region and a second connection hole for exposing a surface of said drain region; and

(k) forming a third conductive film electrically connected to said source region inside said first connection hole, and forming a fourth conductive film electrically connected to said drain region inside said second connection hole.

10.

~~20~~. The method for manufacturing a semiconductor integrated circuit device according to claim 9,

wherein said third conductive film formed inside said first connection hole functions as a part of a source line, and said fourth conductive film formed inside said second connection hole functions as a part of a data line.

21. The method for manufacturing a semiconductor integrated circuit device according to claim 20,

wherein each of said plurality of gate electrodes constitutes a memory cell of a flash memory, and writing into said memory cell is carried out by injecting a charge into said floating gate electrode, and erasing from said memory cell is carried out by discharging, to said semiconductor substrate, said charge injected into said floating gate electrode.

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